## Claims

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- Configuration for the digital-analog conversion of a highfrequency digital input signal (DE) into a carrier-frequency analog output signal (AA),
  - in which a delay device (VZ) has at least one first delay element (VG1) and additional delay elements (VG2,...,VGn) connected downstream from the first in a serially consecutive manner,
- in which the digital input signal (DE) is connected to an input of the first delay element (VG1) and is connected to an input of a first D/A converter (W0),
  - in which the first delay element (VG1) is connected on the output side to an input of another D/A converter (W1) assigned thereto, and, optionally, each additional delay element (VG2,...,VGn) is connected on the output side to an input of another D/A converter (W2,...,Wn) assigned to the respective delay element (VG2,...,VGn),
  - in which all D/A converters (W0,...,Wn) are combined on the output side in a step-by-step manner so that output signals (AS0,...,ASn) of all D/A converters (W0,...,Wn) form the analog output signal (AA), and
  - in which a specific coefficient (k0,...,Kn) is assigned to each each D/A converter (W0,...,Wn) and a specific delay time (τ1,...,τn) is assigned to each delay element (VG2,...,VGn) for the purpose of realizing a filter characteristic,
  - Configuration according to Claim 1, in which an identical clock signal (CLK) is connected to each individual D/A converter (W0,...,Wn).
  - 3. Configuration according to Claim 2, in which the delay times  $(\tau 1, \ldots, \tau n)$  specifically assigned to the delay elements  $(VG1, \ldots, VGn)$  correspond to an entire clock period or to part of the clock

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period of the clock signal (CLK).

- 4. Configuration according to one of the above claims, in which the specific coefficients  $(k0, \ldots, kn)$  and the specific delay times  $(\tau 1, \ldots, \tau n)$  are selected such that a FIR filter characteristic is realized.
- 5. Configuration according to one of the above claims, in which the delay elements (VGl,...,VGn) are configured as D latches timedwith the clock signal (CLK).
  - 6. Configuration according to one of the above claims, in which the D/A converters (W0,...,Wn) are configured as 1-bit D/A converters.
  - 7. Configuration according to one of the above claims, in which the D/A converters (W0,...,Wn) are combined on the output side by means of adding devices (AE1,...,AEn).
- 20 8. Configuration according to one of the above claims, in which the delay times  $(\tau 1, ..., \tau n)$  assigned to the delay elements (VG1, ..., VGn) are identical.
- 9. Configuration according to one of the above claims, in which the output signals (ASO,...,ASn) of the D/A converters (WO,...,Wn) each have a multiple pulse sequence in order to improve the filter function.
- 10. Configuration according to one of the above claims, in which the digital input signal (DE) is broadband.